

## 800G OSFP800 DR8 Specification

### R12OSFP-800G-DR8 / R16OSFP-800G-DR8

#### **Features**

- ◆ Form Factor: Hot-pluggable OSFP800 form factor
- ◆ Data Rate: Aggregate data rate of 850 Gb/s and Breakout data rate of 106.25 Gb/s
- ◆ Optical Interface: Compliant to 2x400GBASE-DR4 and 8x100GBASE-DR
- ◆ Electrical Interface: Compliant to 2x400GAUI-4 and 8x100GAUI-1
- ◆ Management Interface: I2C management interface
- ◆ Reach: Up to 500m over MPO/APC single mode fiber
- ◆ Power consumption: 16 W max
- ◆ Operating case temperature: 0 ~ 70 °C
- ◆ Power Supply: Single 3.3V power supply

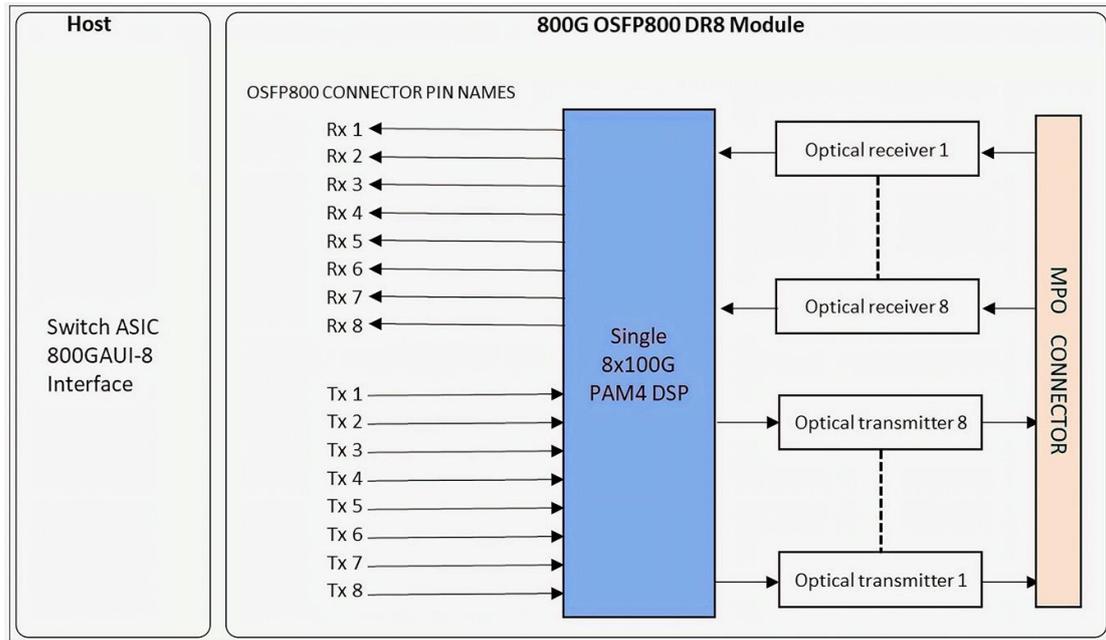
#### **Compliance**

- ◆ Form Factor: OSFP MSA Rev 5.0
- ◆ Optical: IEEE802.3cd /IEEE802.3bs
- ◆ Electrical: IEEE802.3ck
- ◆ Firmware: CMIS 5.2
- ◆ Environment: RoHS
- ◆ Stability: GR-468-CORE

#### **Applications**

- ◆ 800Gb/s Ethernet
- ◆ Data Center

## Functional Block Diagram



### 1. General Description

The 800G OSFP DR8 are high performance, cost effective transceivers designed for utilization in 800 Gigabit Ethernet links over 500 meters. On transmitter side, the module converts eight channels of 53.125 GBaud (PAM4) electrical data to eight channels of parallel optical signals with data rate of 53.125 GBaud (PAM4). At receiver side, the module converts eight channels of parallel optical signals with data rate of 53.125 GBaud (PAM4) into eight channels of 53.125 GBaud(PAM4) electrical output data.

The product is designed according to the OSFP MSA. It is designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

### 2. Absolute Maximum Ratings and Recommended Operating Conditions

(Table 2.1 Absolute Maximum Ratings)

| Parameter                            | Symbol | Min  | Typical | Max | Unit |
|--------------------------------------|--------|------|---------|-----|------|
| Storage Temperature                  | Ts     | -40  |         | 85  | °C   |
| Relative Humidity (non-condensation) | RH     | 15   |         | 85  | %    |
| Supply Voltage                       | Vcc    | -0.5 |         | 3.6 | V    |
| Optical Input Power, per Lane        | PIN    |      |         | 5.0 | dBm  |

(Table 2.2 Recommended Operating Conditions)

| Parameter                  | Symbol | Min   | Typical | Max    | Unit |
|----------------------------|--------|-------|---------|--------|------|
| Operating Case Temperature | TC     | 0     |         | 70     | °C   |
| Signaling Rate, each lane  |        |       | 53.125  |        | GBd  |
| Data Rate Accuracy         |        | -100  |         | 100    | ppm  |
| Power Supply Voltage       | VCC    | 3.135 | 3.3     | 3.465  | V    |
| Pre-FEC Bit Error Ratio    |        |       |         | 2.4E-4 |      |
| Transmission Distance      |        |       |         | 500    | m    |

## 3. Optical Specifications

### 3.1 Optical Transmitter

(Table 3.1 Transmitter optical characteristics)

| Parameter  | Symbol            | Min             | Typical | Max    | Unit |
|--|-------------------|-----------------|---------|--------|------|
| Signaling rate, each lane  | SR                | 53.125+/-100ppm |         |        | GBd  |
| Modulation format  |                   | PAM4            |         |        |      |
| Lane wavelength  | $\lambda$         | 1304.5          | 1311.0  | 1317.5 | nm   |
| Side-mode suppression ratio  | SMSR              | 30              |         |        | dB   |
| Average launch power, each lane <sup>a</sup>                                       | AOP <sub>TX</sub> | -2.9            |         | 4.0    | dBm  |
| Outer Optical Modulation Amplitude (OMA <sub>outer</sub> ), each lane <sup>b</sup> | OMA <sub>TX</sub> | -0.8            |         |        | dBm  |
| Launch power in OMA <sub>outer</sub> minus TDECQ, each lane                        |                   | -2.2            |         |        | dBm  |

|  |                    |     |  |      |       |
|--|--------------------|-----|--|------|-------|
| Transmitter and dispersion eye closure for PAM4, each lane | TDECQ              |     |  | 3.4  | dB    |
| Average launch power of OFF transmitter, each lane         | AOP <sub>OFF</sub> |     |  | -15  | dBm   |
| Extinction ratio, each lane                                | ER                 | 3.5 |  |      | dB    |
| RIN <sub>21.4OMA</sub>                                     |                    |     |  | -136 | dB/Hz |
| Optical return loss tolerance                              | RL <sub>Tol</sub>  |     |  | 21.4 | dB    |
| Transmitter reflectance <sup>c</sup>                       | Reflectance_<br>Tx |     |  | -26  | dB    |

Note:

a. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

b. Even if the TDECQ < 1.4 dB, the OMA<sub>outer</sub> (min) must exceed these values.

c. Transmitter reflectance is defined looking into the transmitter

### 3.2 Optical Receiver

(Table 3.2 Receiver optical characteristics)

| Parameter   | Symbol             | Min             | Typical | Max    | Unit |
|---|--------------------|-----------------|---------|--------|------|
| Signaling rate, each lane   | SR                 | 53.125+/-100ppm |         |        | GBd  |
| Modulation format   |                    | PAM4            |         |        | -    |
| Lane wavelengths  | $\lambda$          | 1304.5          | 1311.0  | 1317.5 | nm   |
| Damage threshold, each lane <sup>a</sup>                                      | DThd               | 5               |         |        | dBm  |
| Average receive power, each lane <sup>b</sup>                                 | AOP <sub>RX</sub>  | -5.9            |         | 4      | dBm  |
| Receiver reflectance  | Reflectance_<br>Rx |                 |         | -26    | dB   |
| Receiver sensitivity (OMA <sub>outer</sub> ), each lane <sup>c</sup>          | RxSens             |                 |         | -4.4   | dBm  |
| Stressed receiver sensitivity (OMA <sub>outer</sub> ), each lane <sup>d</sup> | SRS                |                 |         | -1.9   | dBm  |
| Conditions of stressed receiver sensitivity test: <sup>e</sup>                |                    |                 |         |        |      |
| Stressed eye closure for PAM4 (SECQ), lane under test                         |                    |                 | 3.4     |        | dB   |
| OMA <sub>outer</sub> of each aggressor lane                                   |                    |                 | 4.2     |        | dBm  |
| Rx LOS  | LOS Assert         | LOSA            | -15     | -7.9   | dBm  |
|   | LOS De-assert      | LOSD            |         | -7.4   | dBm  |
|   | LOS Hysteresis     | LOSH            | 0.5     | 5      | dB   |

**Notes:**

- a. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
- b. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
- c. Receiver sensitivity (OMA<sub>outer</sub>), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
- d. Measured with conformance test signal at TP3 for the BER = 2.4E-4.
- e. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

## 4. Electrical and DDM Specifications

### 4.1 Electrical Specifications

(Table 4.1 Module input characteristics)

| Parameter   | Test Point | Min               | Typical | Max  | Unit |
|---|------------|-------------------|---------|------|------|
| Signaling rate, each lane   | TP1        | 53.125 ± 100 ppm  |         |      | GBd  |
| Differential pk-pk voltage tolerance  | TP1a       | 750               |         |      | mV   |
| Peak-to-peak AC common-mode voltage tolerance<br>Low-frequency, VCMLF<br>Full-band, VCMFB | TP1a       | 32<br>80          |         |      | mV   |
| Differential-mode to common-mode return loss, RL <sub>cd</sub>                            | TP1        | Equation (120G-2) |         |      | dB   |
| Effective return loss, ERL  | TP1        | 8.5               |         |      | dB   |
| Differential termination mismatch   | TP1        |                   |         | 10   | %    |
| Module stressed input tolerance   | TP1a       | See 120G.3.4.3    |         |      | -    |
| Single-ended voltage tolerance range  | TP1a       | -0.4              |         | 3.3  | V    |
| DC common-mode voltage tolerance  | TP1        | -0.35             |         | 2.85 | V    |

(Table 4.2 Module output characteristics at TP4)

| Parameter   | Test Point | Min                  | Typical | Max        | Unit |
|---|------------|----------------------|---------|------------|------|
| Signaling rate, each lane   | TP4        | 53.125 ± 100 ppm     |         |            | GBd  |
| Peak-to-peak AC common-mode voltage<br>Low-frequency, VCMLF<br>Full-band, VCMFB | TP4        |                      |         | 32<br>80   | mV   |
| Differential peak-to-peak output voltage<br>Short mode<br>Long mode             | TP4        |                      |         | 600<br>845 | mV   |
| Eye height  | TP4        | 15                   |         |            | mV   |
| Vertical eye closure, VEC   | TP4        |                      |         | 12         | dB   |
| Common-mode to differential-mode<br>return loss, RLdc                           | TP4        | Equation<br>(120G-1) |         |            | dB   |
| Effective return loss, ERL  | TP4        | 8.5                  |         |            | dB   |
| Differential termination mismatch   | TP4        |                      |         | 10         | %    |
| Transition time   | TP4        | 8.5                  |         |            | ps   |
| DC common-mode voltage tolerance  | TP4        | -0.35                |         | 2.85       | V    |

## 4.2 Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

(Table 4.3 Digital Diagnostic Monitor Accuracy)

| Parameter                                      | Accuracy | Unit |
|--|----------|------|
| Internally Measured Transceiver Temperature    | +/-3     | °C   |
| Internally Measured Transceiver Supply Voltage | +/-3     | %    |
| Measured Tx Bias Current                       | +/-10    | %    |
| Measured Tx Output Power                       | +/-3     | dB   |
| Measured Rx Received Average Optical Power     | +/-3     | dB   |

## 5. User Interface

The memory map follows CMIS5.2 and is described as follows:

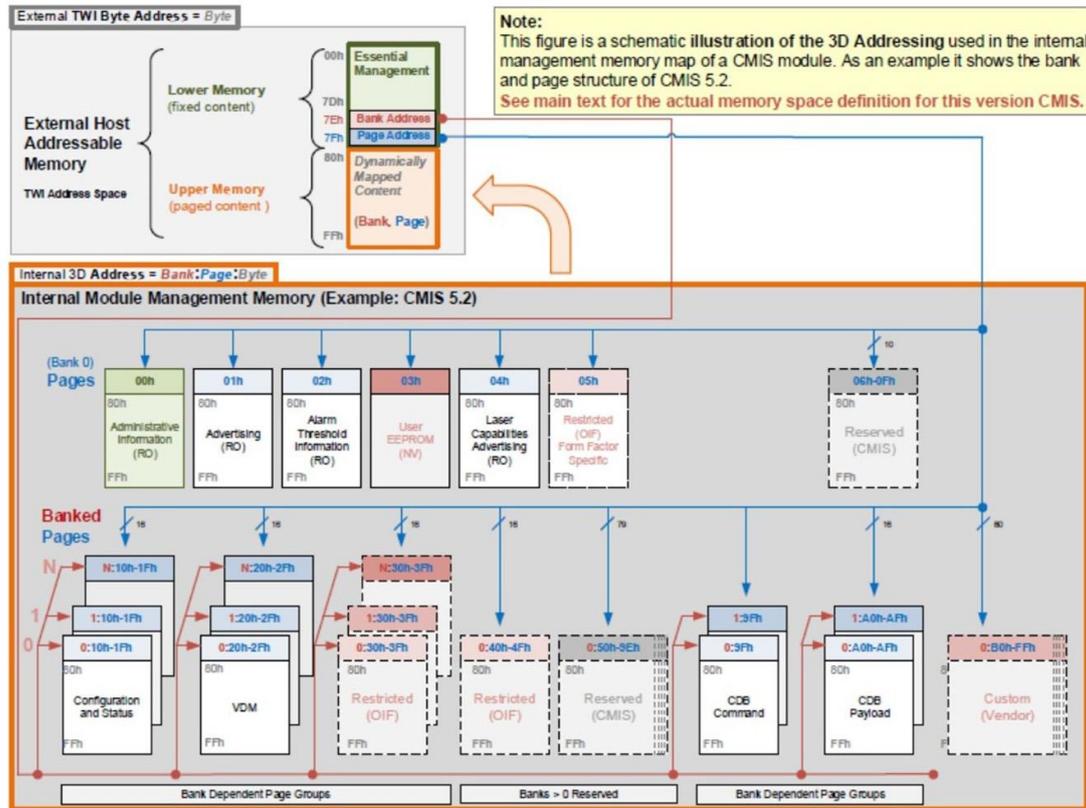
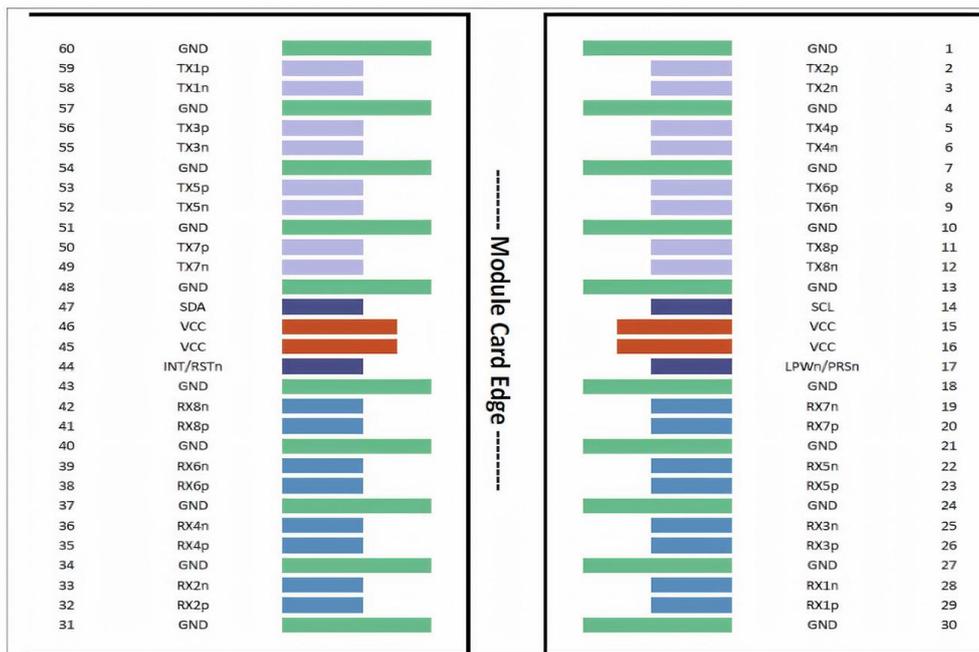


Figure 5.1 CMIS Module Memory Map

## 6. Pin Assignment and Description

The OSFP module pinout and connector pin list are as follows:



(Table 6.1 OSFP connector pin list)

| Pin# | Symbol                 | Description                        | Logic           | Direction       | Plug Sequence <sup>1</sup> | Notes   |
|------|------------------------|------------------------------------|-----------------|-----------------|----------------------------|---|
| 1    | GND                    | Ground                             |                 |                 | 1                          |   |
| 2    | Tx2p                   | Transmitter Data<br>Non-Inverted   | CML-I           | Input from Host | 3                          |   |
| 3    | Tx2n                   | Transmitter Data Inverted          | CML-I           | Input from Host | 3                          |   |
| 4    | GND                    | Ground                             |                 |                 | 1                          |   |
| 5    | Tx4p                   | Transmitter Data<br>Non-Inverted   | CML-I           | Input from Host | 3                          |   |
| 6    | Tx4n                   | Transmitter Data Inverted          | CML-I           | Input from Host | 3                          |   |
| 7    | GND                    | Ground                             |                 |                 | 1                          |   |
| 8    | Tx6p                   | Transmitter Data<br>Non-Inverted   | CML-I           | Input from Host | 3                          |   |
| 9    | Tx6n                   | Transmitter Data Inverted          | CML-I           | Input from Host | 3                          |   |
| 10   | GND                    | Ground                             |                 |                 | 1                          |   |
| 11   | TX8p                   | Transmitter Data<br>Non-Inverted   | CML-I           | Input from Host | 3                          |   |
| 12   | TX8n                   | Transmitter Data Inverted          | CML-I           | Input from Host | 3                          |   |
| 13   | GND                    | Ground                             |                 |                 | 1                          |   |
| 14   | SCL                    | 2-wire Serial interface clock      | LVC MOS-<br>I/O | Bi-directional  | 3                          | Open-Drain<br>with pullup<br>resistor on<br>Host  |
| 15   | VCC                    | +3.3V Power                        |                 | Power from Host | 2                          |   |
| 16   | VCC                    | +3.3V Power                        |                 | Power from Host | 2                          |   |
| 17   | LPWn/PRSn <sup>2</sup> | Low-Power Mode /<br>Module Present | Multi-Level     | Bi-directional  | 3                          | See pin<br>description<br>for required<br>circuit |
| 18   | GND                    | Ground                             |                 |                 | 1                          |   |
| 19   | RX7n                   | Receiver Data Inverted             | CML-O           | Output to Host  | 3                          |   |
| 20   | RX7p                   | Receiver Data Non-Inverted         | CML-O           | Output to Host  | 3                          |   |
| 21   | GND                    | Ground                             |                 |                 | 1                          |   |
| 22   | RX5n                   | Receiver Data Inverted             | CML-O           | Output to Host  | 3                          |   |
| 23   | RX5p                   | Receiver Data Non-Inverted         | CML-O           | Output to Host  | 3                          |   |
| 24   | GND                    | Ground                             |                 |                 | 1                          |   |
| 25   | RX3n                   | Receiver Data Inverted             | CML-O           | Output to Host  | 3                          |   |
| 26   | RX3p                   | Receiver Data Non-Inverted         | CML-O           | Output to Host  | 3                          |   |
| 27   | GND                    | Ground                             |                 |                 | 1                          |   |
| 28   | RX1n                   | Receiver Data Inverted             | CML-O           | Output to Host  | 3                          |   |
| 29   | RX1p                   | Receiver Data Non-Inverted         | CML-O           | Output to Hos   | 3                          |   |
| 30   | GND                    | Ground                             |                 |                 | 1                          |   |

|    |                       |                                 |             |                 |   |  |
|----|-----------------------|---------------------------------|-------------|-----------------|---|--|
| 31 | GND                   | Ground                          |             |                 | 1 |  |
| 32 | RX2p                  | Receiver Data Non-Inverted      | CML-O       | Output to Host  | 3 |  |
| 33 | RX2n                  | Receiver Data Inverted          | CML-O       | Output to Host  | 3 |  |
| 34 | GND                   | Ground                          |             |                 | 1 |  |
| 35 | RX4p                  | Receiver Data Non-Inverted      | CML-O       | Output to Host  | 3 |  |
| 36 | RX4n                  | Receiver Data Inverted          | CML-O       | Output to Host  | 3 |  |
| 37 | GND                   | Ground                          |             |                 | 1 |  |
| 38 | RX6p                  | Receiver Data Non-Inverted      | CML-O       | Output to Host  | 3 |  |
| 39 | RX6n                  | Receiver Data Inverted          | CML-O       | Output to Host  | 3 |  |
| 40 | GND                   | Ground                          |             |                 | 1 |  |
| 41 | RX8p                  | Receiver Data Non-Inverted      | CML-O       | Output to Host  | 3 |  |
| 42 | RX8n                  | Receiver Data Inverted          | CML-O       | Output to Host  | 3 |  |
| 43 | GND                   | Ground                          |             |                 | 1 |  |
| 44 | INT/RSTn <sup>3</sup> | Module Interrupt / Module Reset | Multi-Level | Bi-directional  | 3 | See pin description for required circuit |
| 45 | VCC                   | +3.3V Power                     |             | Power from Host | 2 |  |
| 46 | VCC                   | +3.3V Power                     |             | Power from Host | 2 |  |
| 47 | SDA                   | 2-wire Serial interface data    | LVC MOS-I/O | Bi-directional  | 3 | Open-Drain with pullup resistor on Host  |
| 48 | GND                   | Ground                          |             |                 | 1 |  |
| 49 | TX7n                  | Transmitter Data Inverted       | CML-I       | Input from Host | 3 |  |
| 50 | TX7p                  | Transmitter Data Non-Inverted   | CML-I       | Input from Host | 3 |  |
| 51 | GND                   | Ground                          |             |                 | 1 |  |
| 52 | TX5n                  | Transmitter Data Inverted       | CML-I       | Input from Host | 3 |  |
| 53 | TX5p                  | Transmitter Data Non-Inverted   | CML-I       | Input from Host | 3 |  |
| 54 | GND                   | Ground                          |             |                 | 1 |  |
| 55 | TX3n                  | Transmitter Data Inverted       | CML-I       | Input from Host | 3 |  |
| 56 | TX3p                  | Transmitter Data Non-Inverted   |             |                 | 3 |  |
| 57 | GND                   | Ground                          |             |                 | 1 |  |
| 58 | TX1n                  | Transmitter Data Inverted       | CML-I       | Input from Host | 3 |  |
| 59 | TX1p                  | Transmitter Data Non-Inverted   | CML-I       | Input from Host | 3 |  |
| 60 | GND                   | Ground                          |             |                 | 3 |  |

## Notes:

1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is 1,2,3.

- 2. LPWn/PRSn is a multi-level signal for low power control from host to module and module presence indication from module to host. It designed according to OSFP Module Specification Section 13.5.3
- 3. INT/RSTn is a multi-level signal for interrupt request from module to host and reset control from host to module. It designed

## 7. Mechanical Dimensions

Package dimensions in mm are specified in OSFP MSA.

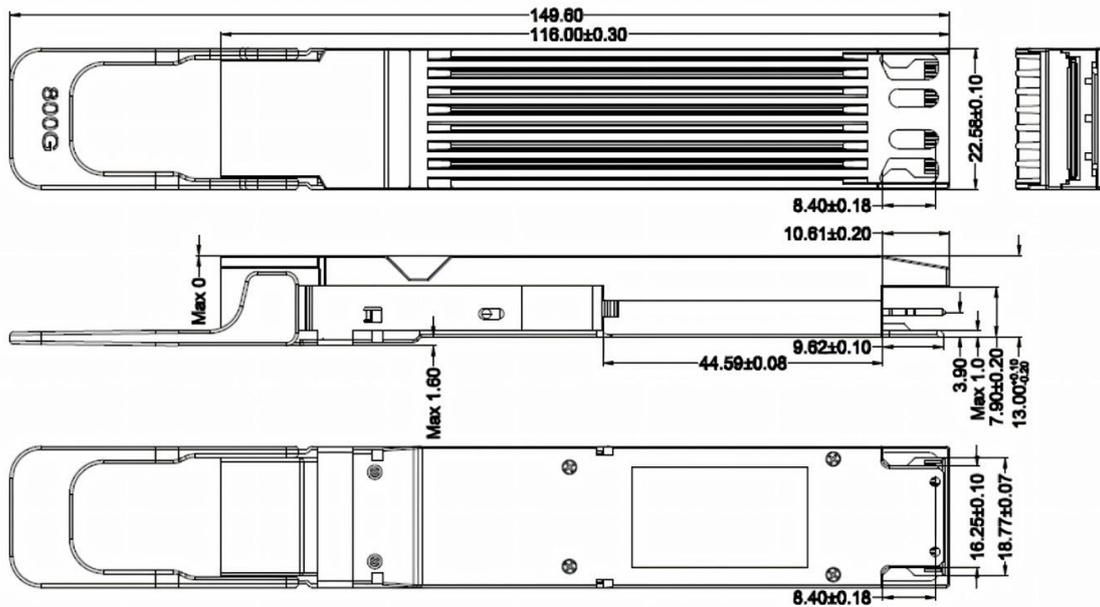


Figure 7.1 Package dimensions

## 8. Ordering Information

| Part Number      | Temperature Range | Distance | Media Connector | Fiber Type | E/O      | O/E     |
|------------------|-------------------|----------|-----------------|------------|----------|---------|
| R12OSFP-800G-DR8 | 0 to 70°C         | 500m     | Dual MPO-12     | SMF        | Siph PIC | Siph PD |
| R16OSFP-800G-DR8 | 0 to 70°C         | 500m     | MPO-16          | SMF        | Siph PIC | Siph PD |